

AMENDMENTS TO THE CLAIMS:

Please cancel claims 1-16, 21-30, 33, 36 and 39, without prejudice. Kindly amend claims 31 and 32, and add new claims 42 and 43, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claims 1-30 (canceled)

Claim 31 (currently amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode;

an interlayer insulation film covering said gate electrode; and

a contact formed in said interlayer insulation film and being in contact with a top surface and a side surface of said visor portion, said side wall and said diffusion layer formed on a top surface of said semiconductor substrate,

wherein said visor portion has no overhang with respect to said side wall.

Claim 32 (currently amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; ~~and~~

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode, said side wall being formed of a lamination of at least two insulation films having different etching properties, wherein said visor portion has no overhang with respect to said side wall; and

a contact formed in said interlayer insulation film and being in contact with a top surface and a side surface of said visor portion, said side wall and said diffusion layer formed on a top surface of said semiconductor substrate.

Claim 33 (canceled)

Claim 34 (previously presented): The semiconductor device according to claim 31, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

Claim 35 (previously presented): The semiconductor device according to claim 32, wherein said gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

Claim 36 (canceled)

HAYES SOLOWAY P.C.
130 W. CUSHING ST.
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Claim 37 (previously presented): The semiconductor device according to claim 34, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Claim 38 (previously presented): The semiconductor device according to claim 35, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part.

Claim 39 (canceled)

Claim 40 (previously presented): The semiconductor device according to claim 37, wherein a side surface of said upper part forms a tapered slope.

Claim 41 (previously presented): The semiconductor device according to claim 38, wherein a side surface of said upper part forms a tapered slope.

Claim 42 (new): The semiconductor device according to claim 31, wherein said gate electrode is a gate electrode of one transistor and said diffusion layer is a diffusion layer of a drain or source of another transistor.

Claim 43 (new): The semiconductor device according to claim 32, wherein said gate electrode is a gate electrode of one transistor and said diffusion layer is a diffusion layer of a drain or source of another transistor.

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TEL. 603.668.1400
FAX. 603.668.8567